TGA2753-SM

5.9 – 7.7 GHz Power Amplifier

Applications

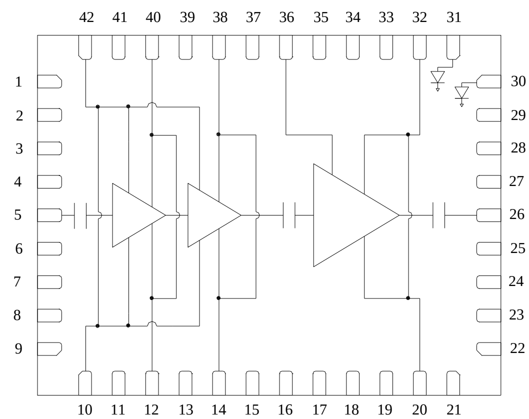
- Point-to-Point Radio
- Linear C-band Sat-Com

42 lead 7x9mm QFN package

Product Features

- Frequency Range: 5.9 – 7.7 GHz
- Power: 40 dBm Psat
- Gain: 31 dB
- TOI: 47 dBm at 30 dBm/tone
- Integrated Power Detector
- Bias: Vd1 = Vd2 = 6 V, Id1 + Id2 = 1000 mA, Vd3 = 28V, Id3 = 190mA
- Package Dimensions: 7.0 x 9.0 x 0.9 mm

Functional Block Diagram



General Description

The TriQuint TGA2753-SM is a C-Band Power Amplifier with integrated power detector. The TGA2753-SM operates from 5.9 – 7.7 GHz and is designed using TriQuint's power GaAs pHEMT and GaN HEMT production processes.

The TGA2753-SM typically provides 40 dBm of saturated output power with small signal gain of 31 dB. Third Order Intercept is 47 dBm at 30 dBm SCL.

The TG2753-SM is available in a low-cost, surface mount 42 lead 7x9 QFN package and is ideally suited for Point-to-Point Radio.

Lead-free and RoHS compliant

Pin Configuration

Pin No.	Label
1, 2, 3, 4, 6, 7, 8, 9,11, 13, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 27, 28, 29, 33, 34, 35, 37, 39, 41	NC
5	RF IN
10, 42	Vg12
12, 40	Vd1
14, 38	Vd2
20, 32	Vd3
26	RF OUT
30	Vref
31	Vdet
36	Vg3

Ordering Information

Part No.	ECCN	Description
TGA2753-SM	3A001.b.2.b.1	5.9 – 7.7 GHz 10W Amp

Standard T/R size = 500 pieces on a 7" reel

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage,Vd1, Vd2	9 V
Drain Voltage,Vd3	32 V
Drain Current, Id1 + Id2	2443 mA
Drain Current, Id3	825 mA
Power Dissipation, Driver Stages, Pdiss	7.2 W
Power Dissipation, Final Stage, Pdiss	17 W
RF Input Power, CW, 50Ω, T = 25ºC	29 dBm
GaAs Channel Temperature, Tch	200 °C
GaN Channel Temperature, Tch	275 °C
Mounting Temperature (30 Seconds)	260 ºC
Storage Temperature	-40 to 150 ºC

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating

Parameter	Min	Typ	Max	Units
Operating Temp. Range	-40	+25	+85	°C
Vd1, Vd2		6		V
Vd3		28		V
Id1 + Id2		1000		mA
Id3		190		mA
Vg12		-0.7		V
Vg3		-2.6		V
Id1 + Id2 drive (at 34 dBm Pout)		1040		mA
Id3 drive (at 34 dBm Pout)		470		mA

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

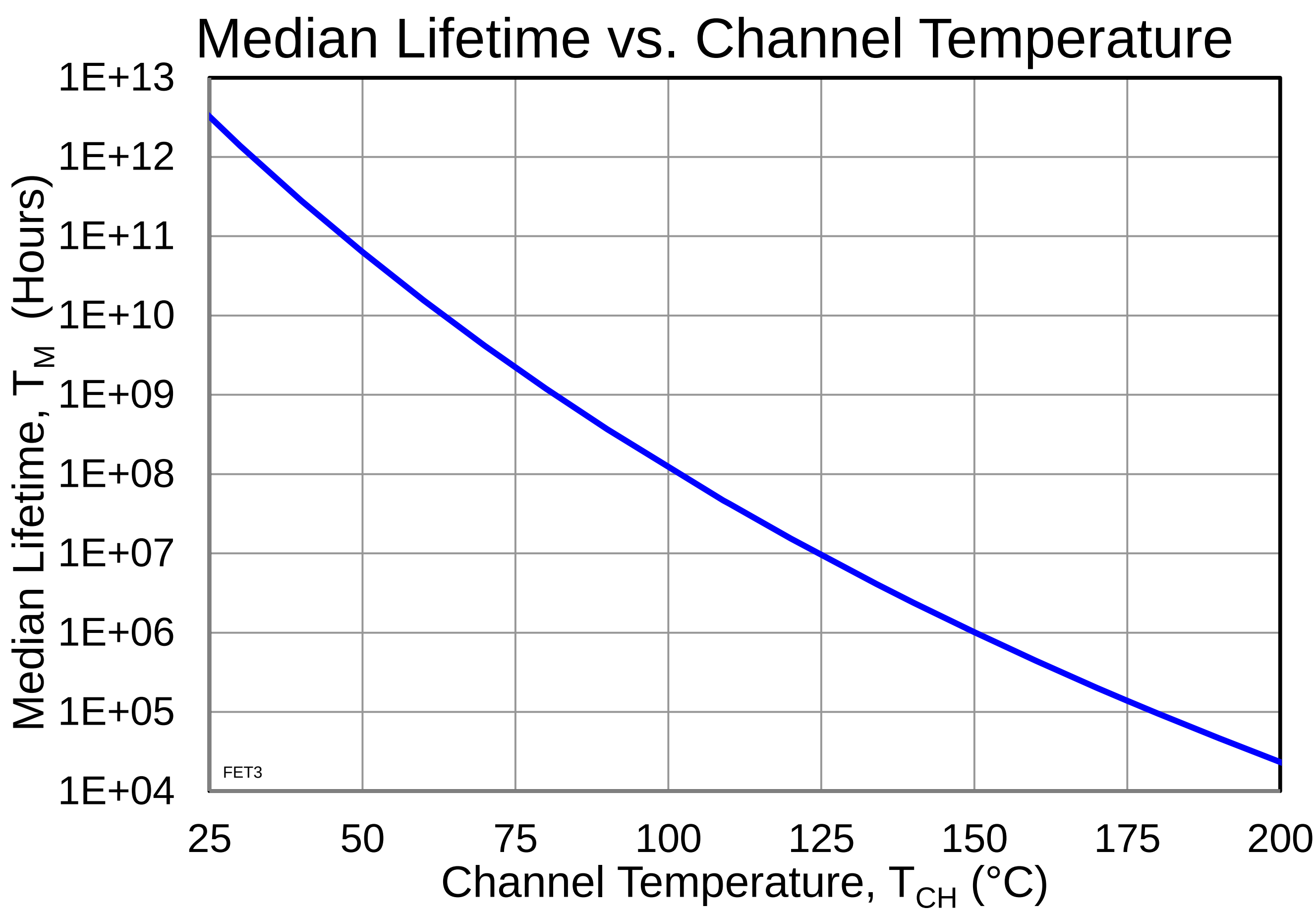
Test conditions unless otherwise noted: Vd1 = Vd2 = +6 V, Id1 + Id2 = 1000 mA, Vg12 =-0.7 V, Vd3 = +28V, Id3 = 190 mA, Vg3 = -2.6V, Temp= +25°C, Z_0 = 50 Ω

Parameter	Min	Typ	Max	Units
RF Frequency Range	5.9		7.7	GHz
Small Signal Gain		31		dB
Input Return Loss, IRL		5		dB
Output Return Loss, ORL		12		dB
Output Power at Pin = 12 dBm		40		dBm
Output Third Order Intercept, TOI @ 30 dBm/Tone		47		dBm
Power Added Efficiency		30		%
Gain Temperature Coefficient		-0.04		dB/°C
Power Temperature Coefficient		-0.013		dBm/°C

Specifications

Thermal and Reliability Information (Driver Stages)

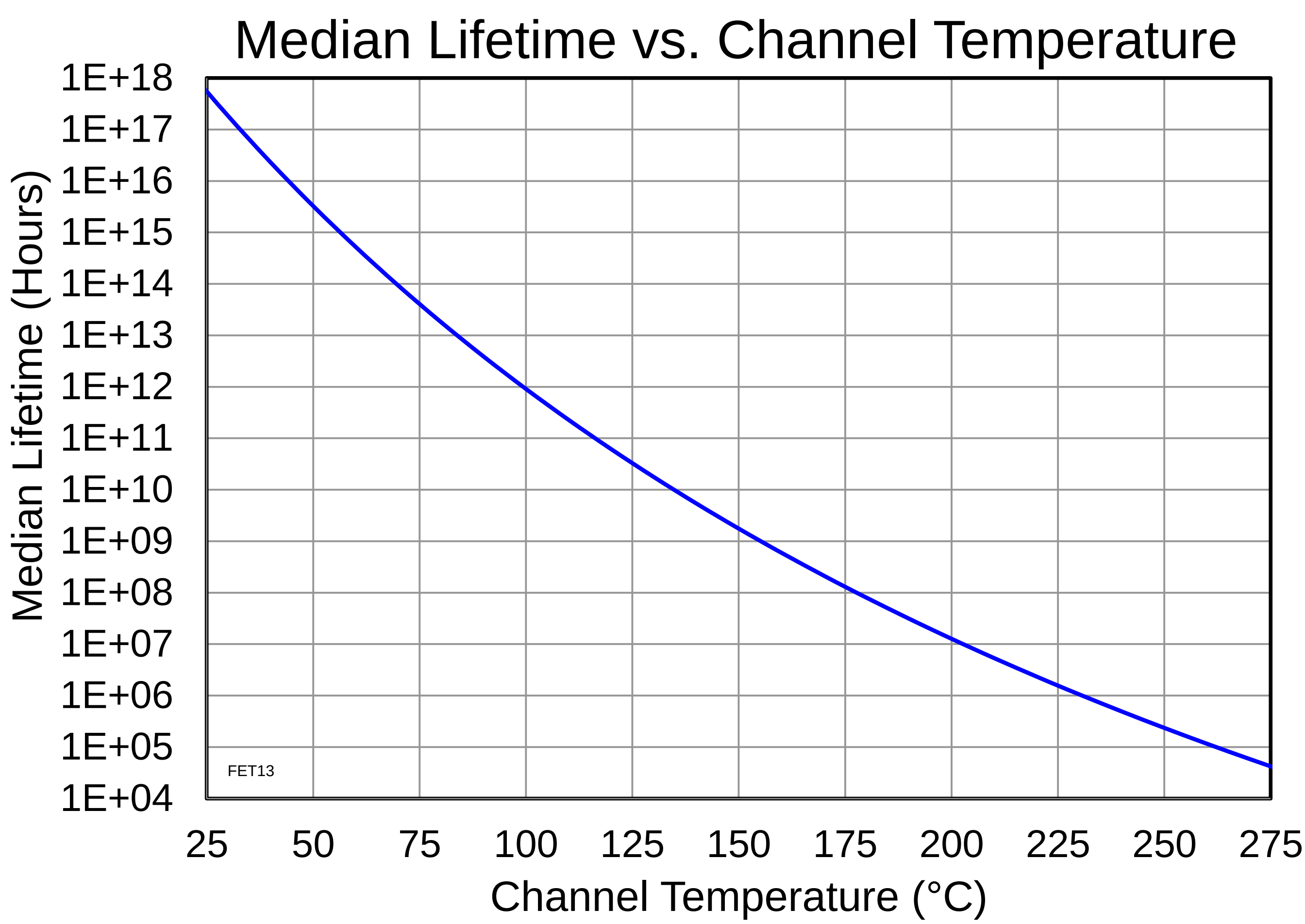
Parameter	Conditions	Rating
Thermal Resistance, θ_{JC}, measured to back of package	Tbase = 85 °C	θ_{JC_driver} = 9 °C/W
Channel Temperature (Tch), and Median Lifetime (Tm)	Tbase = 85 °C $Vd_{\_driver}$ = 6 V, $Id_{\_driver}$ = 1000 mA $Pdiss_{\_driver}$ = 6 W	$Tch_{\_driver}$ = 139 °C $Tm_{\_driver}$ = 2.6E+6 Hours
Channel Temperature (Tch), and Median Lifetime (Tm) at 34 dBm Pout	Tbase = 85 °C $Vd_{\_driver}$ = 6 V, $Id_{\_driver}$ = 1040 mA $Pdiss_{\_driver}$ = 6.2 W	$Tch_{\_driver}$ = 142 °C $Tm_{\_driver}$ = 1.3E+6 Hours



Specifications

Thermal and Reliability Information (Final Stage)

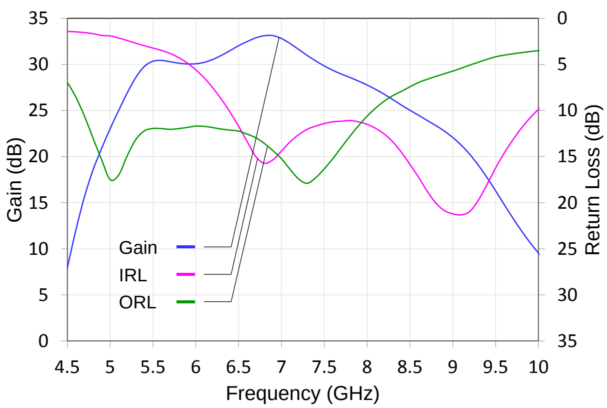
Parameter	Conditions	Rating
Thermal Resistance, θ_{JC}, measured to back of package	Tbase = 85 °C	θ_{JC_final} = 8.2 °C/W
Channel Temperature (Tch), and Median Lifetime (Tm)	Vd_final = 28 V, Id_final = 190 mA Pdiss_final = 5.3 W	Tch_final = 129 °C Tm_final = 2.01E+10 Hours
Channel Temperature (Tch), and Median Lifetime (Tm) at 34 dBm Pout	Vd_final = 28 V, Id_final = 470 mA Pdiss_final = 13.2 W	Tch_final = 193 °C Tm_final = 2.37E+7 Hours



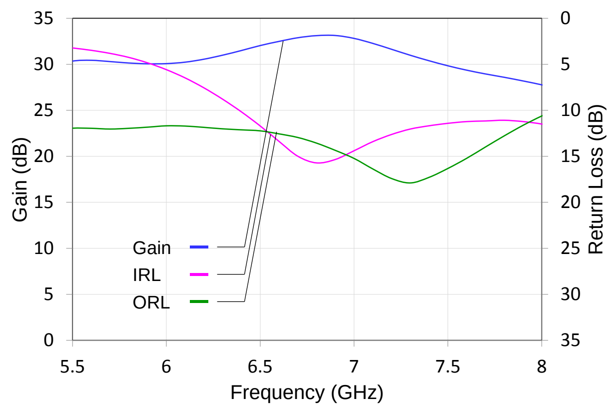
Typical Performance

Test conditions unless otherwise noted: Vd1 = Vd2 = +6 V, Id1 + Id2 = 1000 mA, Vg12 =-0.7 V, Vd3 = +28V, Id3 = 190 mA, Vg3 = -2.6V, Temp= +25°C, Z_0 = 50 Ω

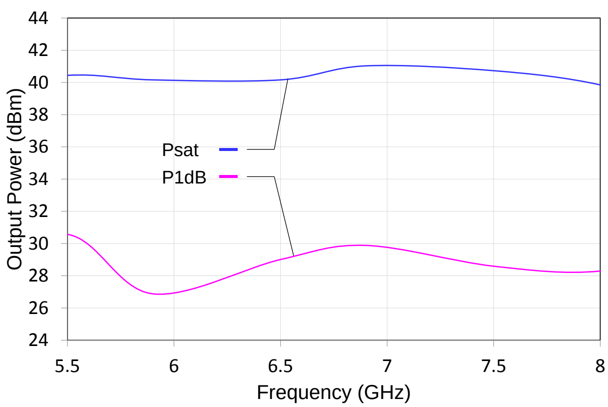
S-Parameter vs. Frequency



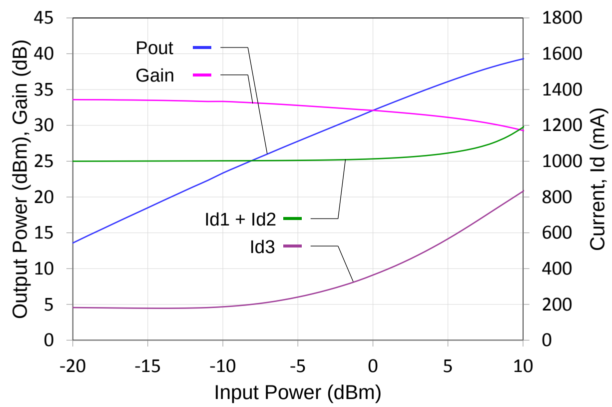
S-Parameter vs. Frequency



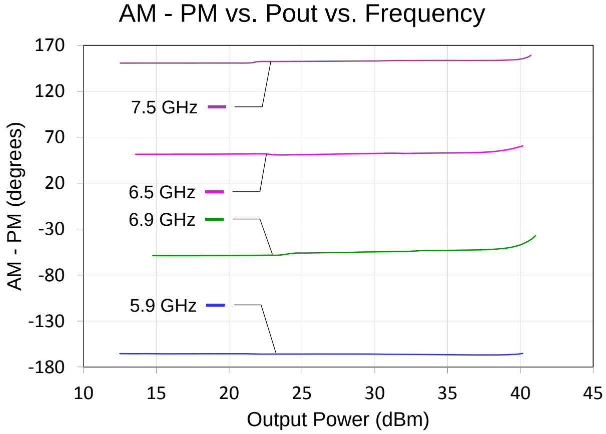
Output Power vs. Frequency



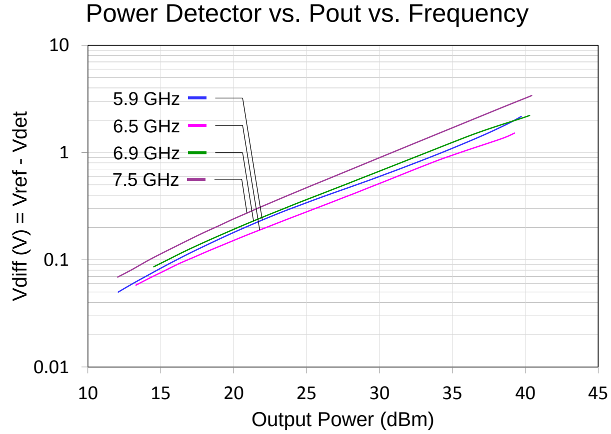
Pout, Gain, Id vs. Pin @ 6.5 GHz



AM - PM vs. Pout vs. Frequency

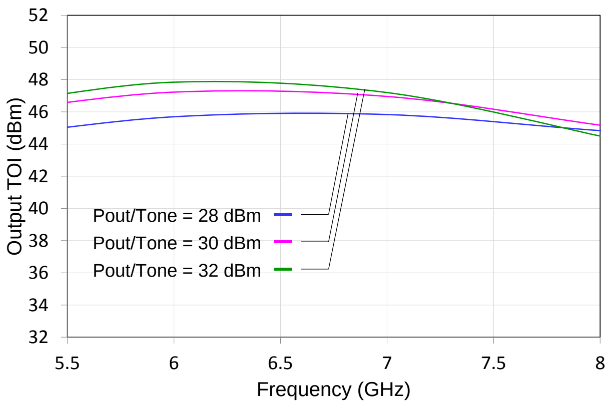


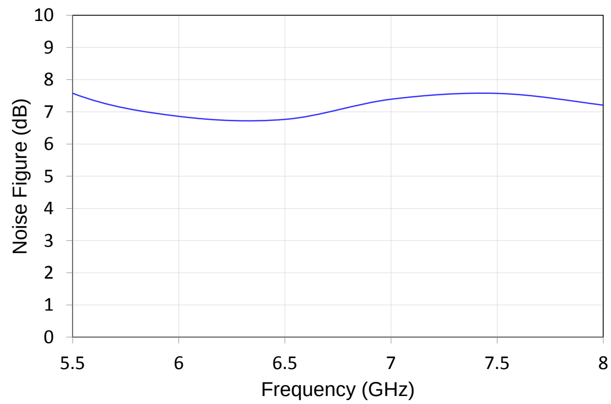
Power Detector vs. Pout vs. Frequency

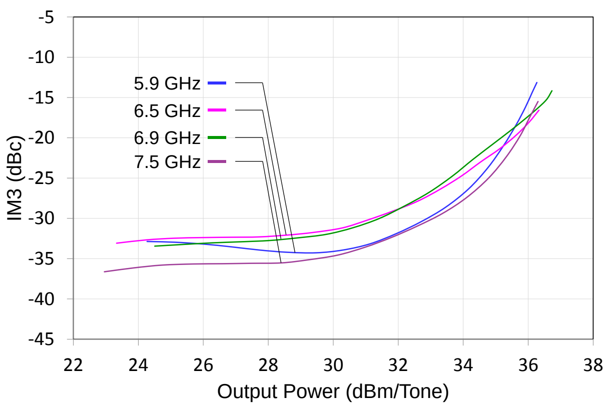


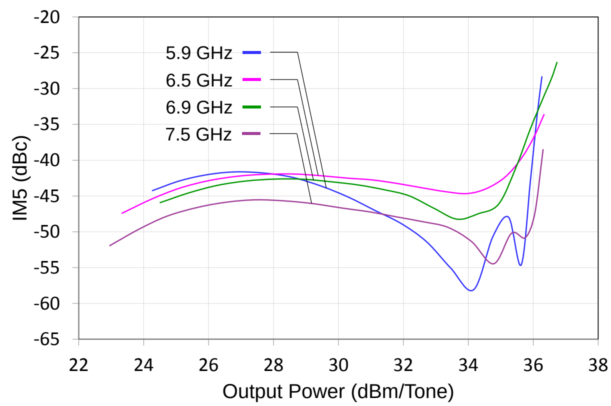
Typical Performance

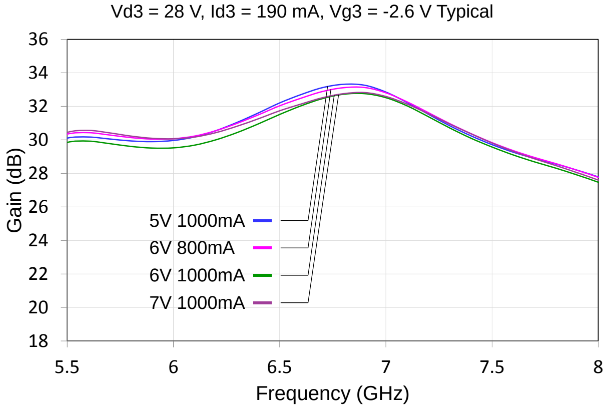
Test conditions unless otherwise noted: Vd1 = Vd2 = +6 V, Id1 + Id2 = 1000 mA, Vg12 =-0.7 V, Vd3 = +28V, Id3 = 190 mA, Vg3 = -2.6V, Temp= +25°C, Z_0 = 50 Ω

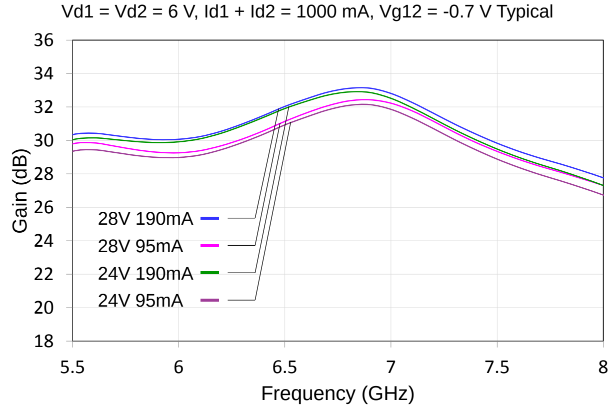








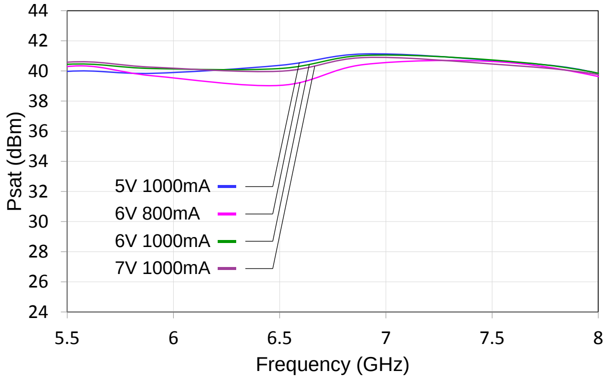




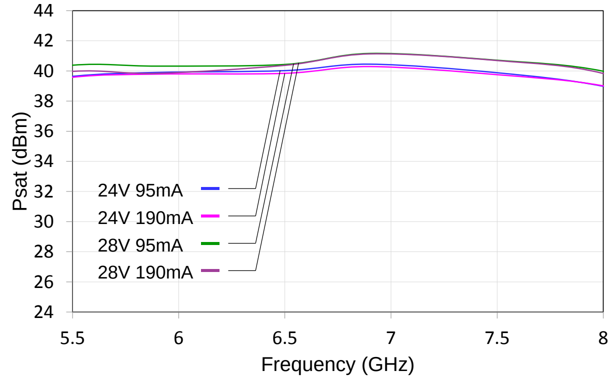
Typical Performance

Test conditions unless otherwise noted: Vd1 = Vd2 = +6 V, Id1 + Id2 = 1000 mA, Vg12 =-0.7 V, Vd3 = +28V, Id3 = 190 mA, Vg3 = -2.6V, Temp= +25°C, Z_0 = 50 Ω

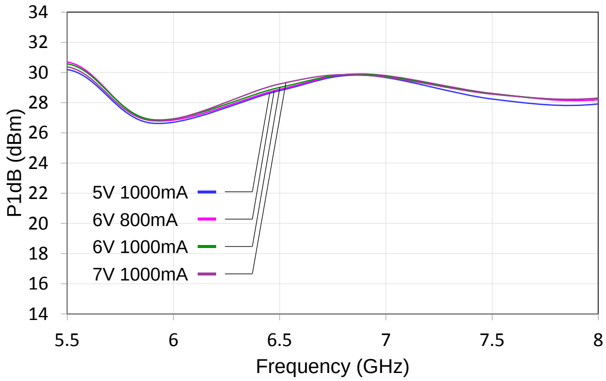
Psat vs. Frequency vs. Bias (Vd1 and Vd2)
Vd3 = 28 V, Id3 = 190 mA, Vg3 = -2.6 V Typical



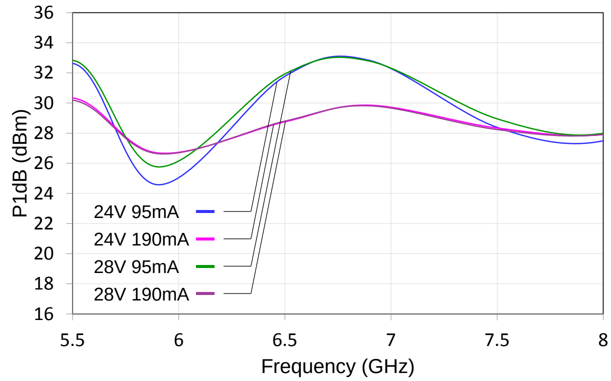
Psat vs. Frequency vs. Bias (Vd3)
Vd1 = Vd2 = 6 V, Id1 + Id2 = 1000 mA, Vg12 = -0.7 V Typical



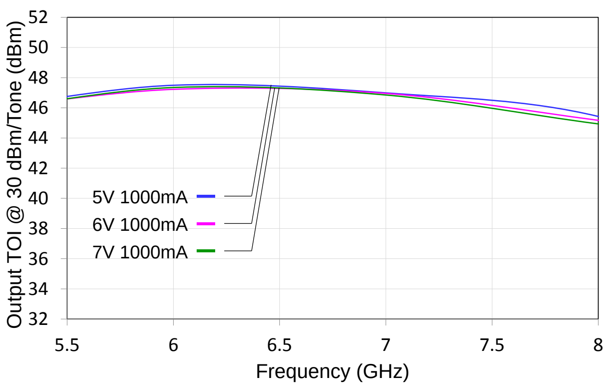
P1dB vs. Frequency vs. Bias (Vd1 and Vd2)
Vd3 = 28 V, Id3 = 190 mA, Vg3 = -2.6 V Typical



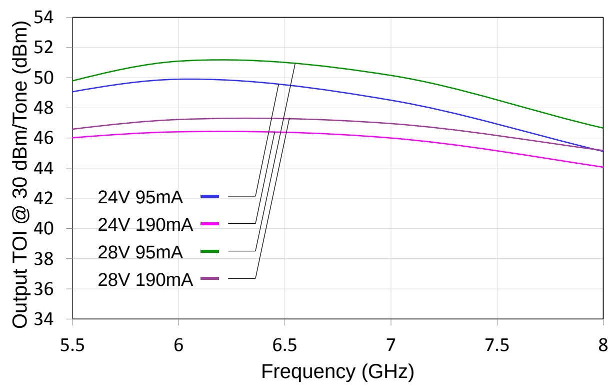
P1dB vs. Frequency vs. Bias (Vd3)
Vd1 = Vd2 = 6 V, Id1 + Id2 = 1000 mA, Vg12 = -0.7 V Typical



TOI vs. Frequency vs. Bias (Vd1 and Vd2)
Vd3 = 28 V, Id3 = 190 mA, Vg3 = -2.6 V Typical



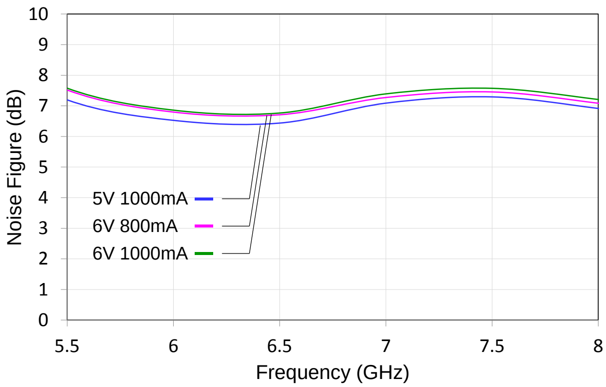
TOI vs. Frequency vs. Bias (Vd3)
Vd1 = Vd2 = 6 V, Id1 + Id2 = 1000 mA, Vg12 = -0.7 V Typical



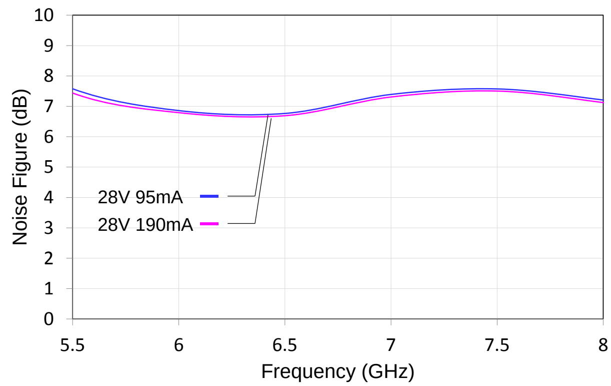
Typical Performance

Test conditions unless otherwise noted: Vd1 = Vd2 = +6 V, Id1 + Id2 = 1000 mA, Vg12 =-0.7 V, Vd3 = +28V, Id3 = 190 mA, Vg3 = -2.6V, Temp= +25°C, Z_0 = 50 Ω

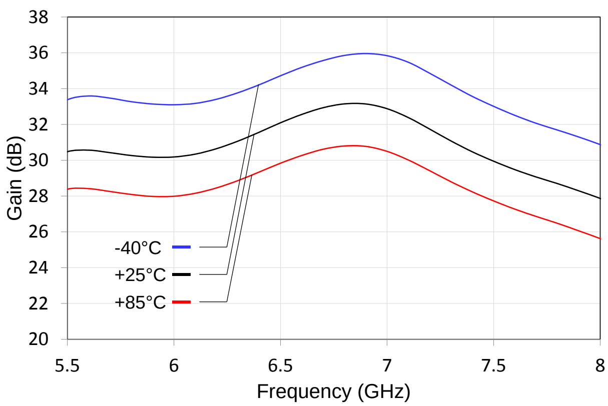
Noise Figure vs. Frequency vs. Bias (Vd1 and Vd2)
Vd3 = 28 V, Id3 = 190 mA, Vg3 = -2.6 V Typical



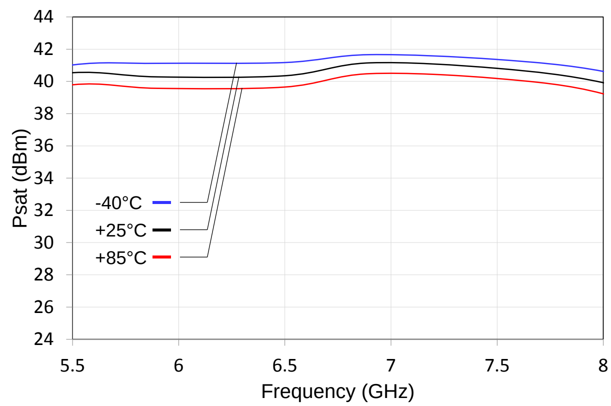
Noise Figure vs. Frequency vs. Bias (Vd3)
Vd1 = Vd2 = 6 V, Id1 + Id2 = 1000 mA, Vg12 = -0.7 V Typical



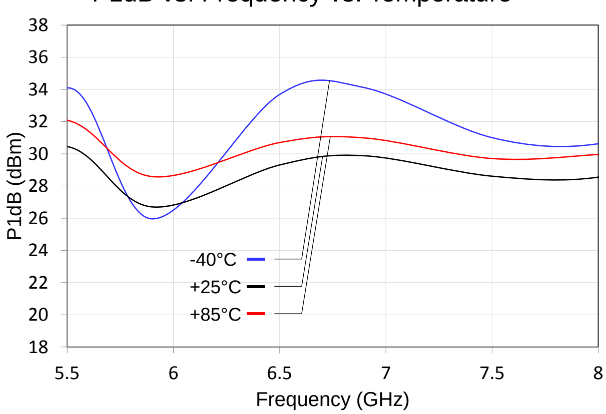
Gain vs. Frequency vs. Temperature



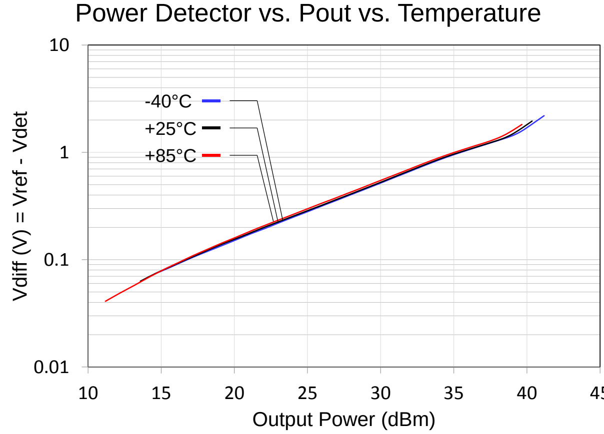
Psat vs. Frequency vs. Temperature



P1dB vs. Frequency vs. Temperature

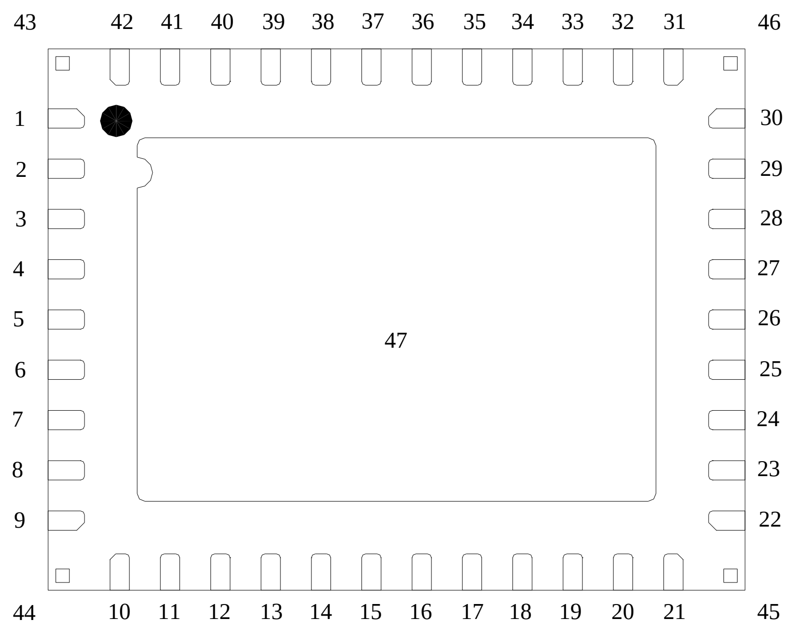


Power Detector vs. Pout vs. Temperature



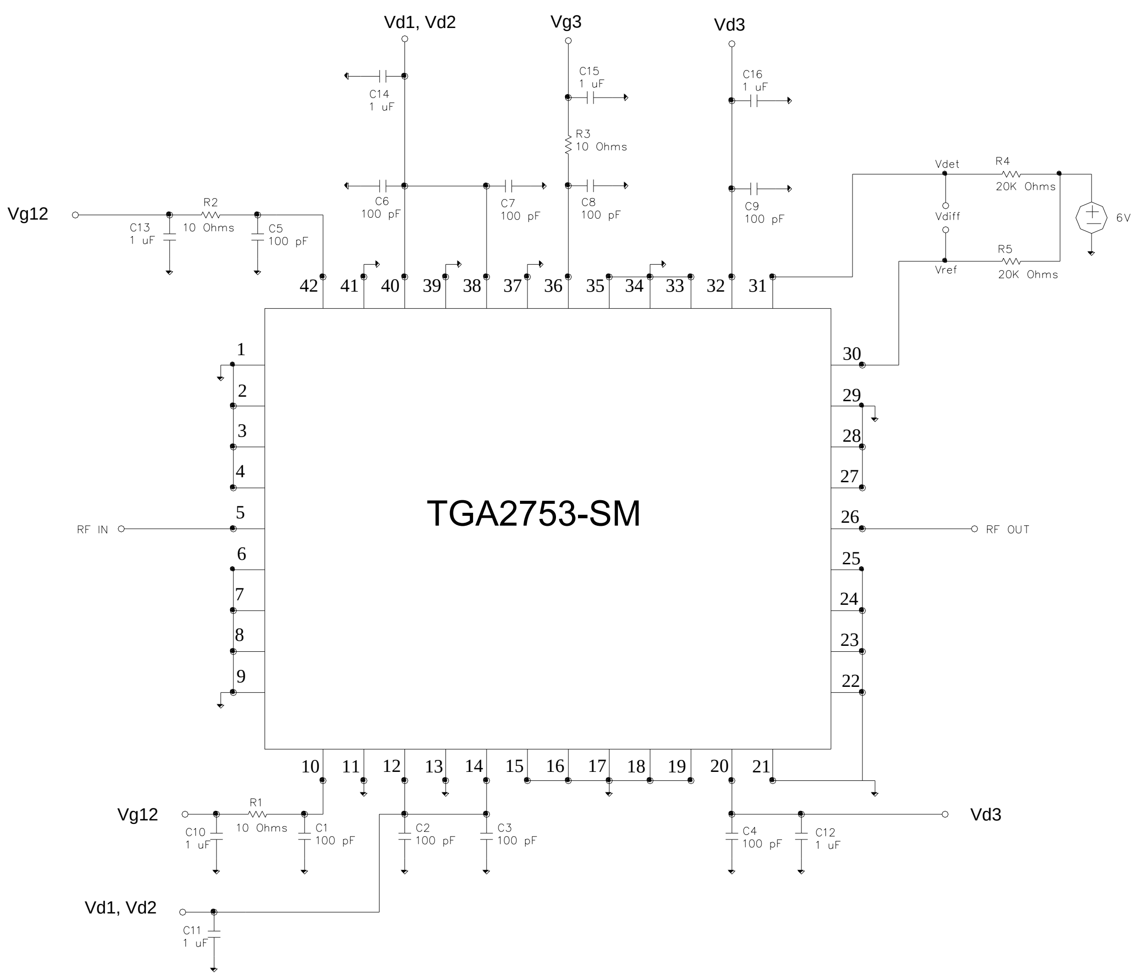
Pin Configuration and Description

Top View



Pin No.	Label	Description
1, 2, 3, 4, 6, 7, 8, 9,11, 13, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 27, 28, 29, 33, 34, 35, 37, 39, 41	NC	No internal connection; must be grounded on PCB.
5	RF IN	RF Input, matched to 50 ohms, AC Coupled.
10, 42	Vg12	Gate voltage. Bias network is required; can be biased from either pin, and non-biased pin can be left open; see Application Circuit on page 11 as an example.
12, 40	Vd1	Drain voltage. Bias network is required; see Application Circuit on page 11 as an example.
14, 38	Vd2	Drain voltage. Bias network is required; see Application Circuit on page 11 as an example.
20, 32	Vd3	Drain voltage. Bias network is required; see Application Circuit on page 11 as an example.
26	RF OUT	RF Output, matched to 50 ohms, AC Coupled.
30	Vref	Reference diode output voltage.
31	Vdet	Detector diode output voltage. Varies with RF output power.
36	Vg3	Gate voltage. Bias network is required; see Application Circuit on page 11 as an example.
43, 44, 45, 46, 47	GND	Backside Paddle. Multiple vias should be employed to minimize inductance and thermal resistance; see Mounting Configuration on page 14 for suggested footprint.

Application Circuit



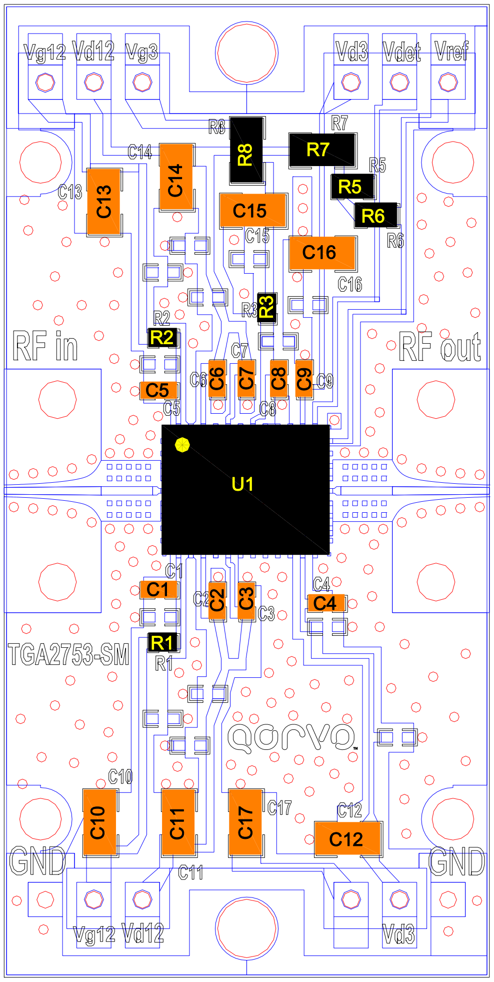
Vg12 can be biased from either side (pin 10 or pin 42), and the non-biased side can be left open.
Vd1, Vd2, and Vd3 must be biased from both sides.

Bias-up Procedure	Bias-down Procedure
Vg12 set to -1.5 V	Turn off RF signal
Vg3 set to -3.5 V	Reduce Vg12 to -1.5V. Ensure Id ~ 0 mA
Vd1, Vd2 set to 6 V	Reduce Vg3 to -3.5V. Ensure Id ~ 0 mA
Vd3 set to 28 V	Turn Vd1, Vd2, Vd3 to 0 V
Adjust Vg12 more positive until quiescent Id is 1000 mA. This will be ~ Vg = -0.7 V typical	Turn Vg12, Vg3 to 0 V
Adjust Vg3 more positive until quiescent Id is 190 mA. This will be ~ Vg = -2.6 V typical	
Apply RF signal	

Application Circuit

PC Board Layout

Board material is RO4003 0.008” thickness with ½ oz copper cladding.
For further technical information, refer to the TGA2753-SM Product Information page.



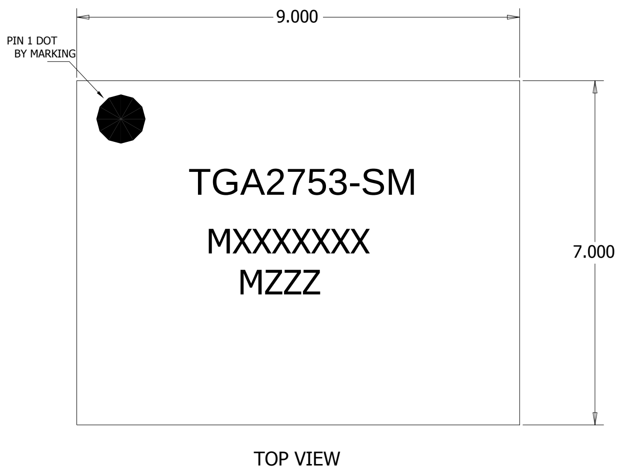
Bill of Material

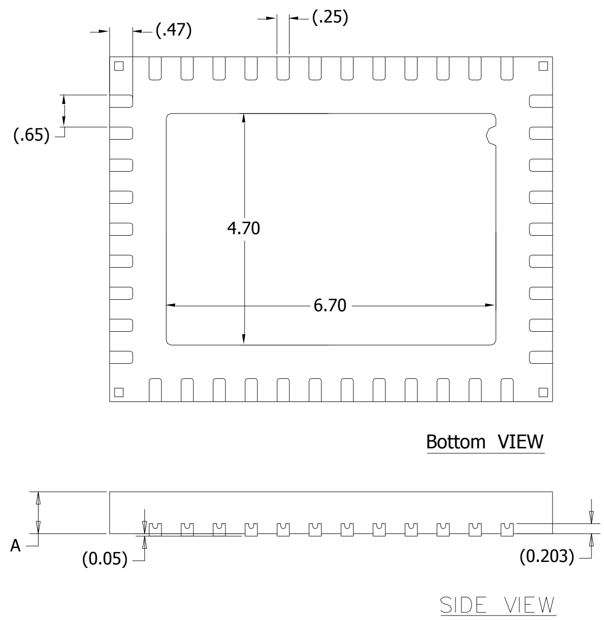
Ref Des	Value	Description	Manufacturer	Part Number
C1 – C9	100 pF	Cap, 0402, 50V, 5%, C0G	various	
C10 – C17	1 µF	Cap, 0603, 50V, 5%, X5R	various	
R1 – R3	10 Ω	Res, 0402, 1/16W, 5%, SMD	various	
R5, R6	20 KΩ	Res, 0603, 1/16W, 5%, SMD	various	
R7, R8	0 Ω	Res, 0805, 1/16W, 5%, SMD	various	
U1		5.9 – 7.7 GHz Power Amplifier	Triquint	TGA2753-SM

Mechanical Information

Package Marking and Dimensions

All dimensions are in millimeters.





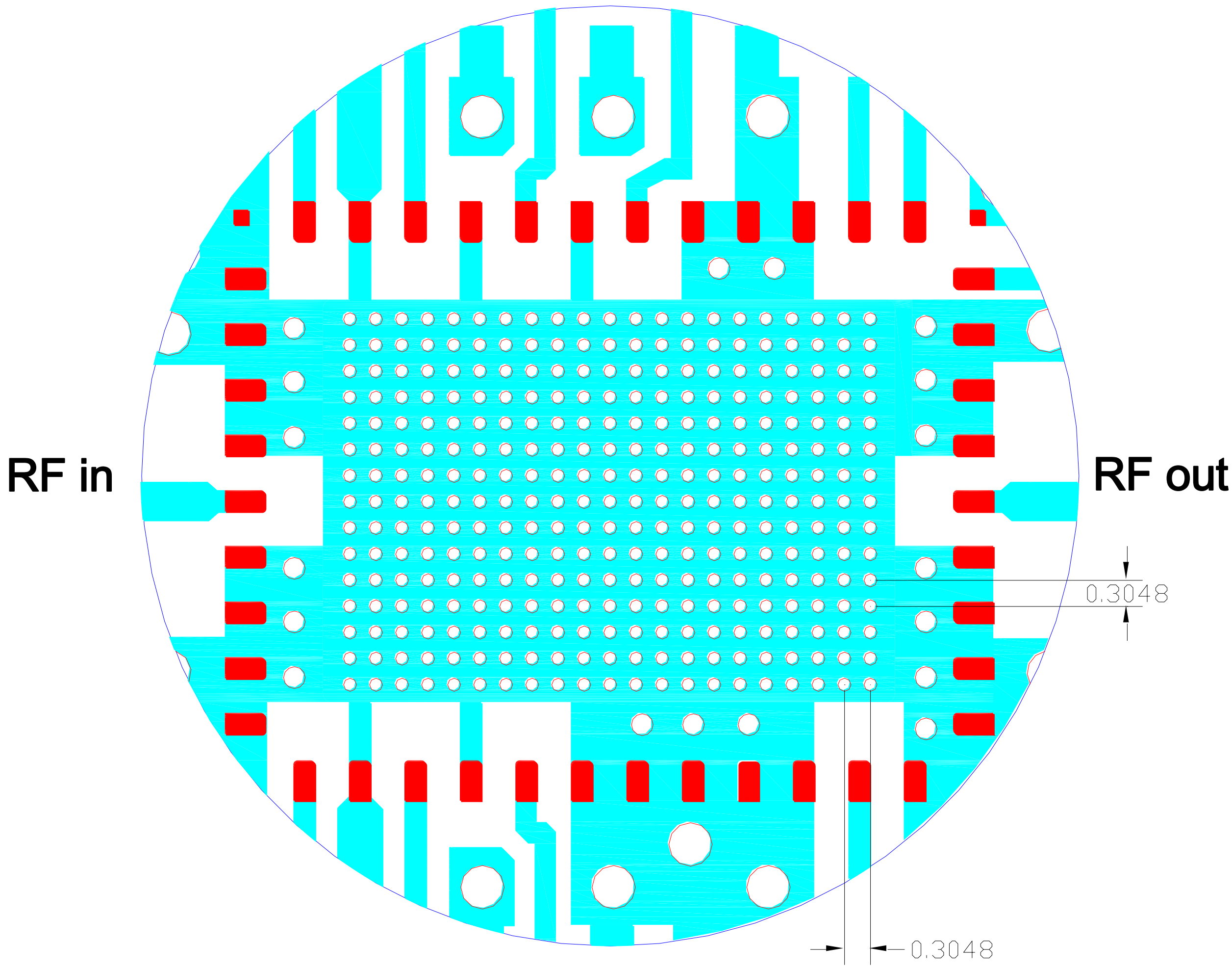
		SLP
A	MAX.	0.900
	NOM.	0.850
	MIN.	0.800

The TGA2753-SM will be marked with the “TGA2753-SM” designator and a lot code marked below the part designator. The “MXXXXXXX” represents the lot number. The “ZZZ” is a unique serial number.

This package is lead-free/RoHS-compliant with a copper alloy base (CDA194), and the plating material on the leads is NiPdAu. It is compatible with lead-free (maximum 260 °C reflow temperature) soldering process.

Mechanical Information

PCB Mounting Pattern



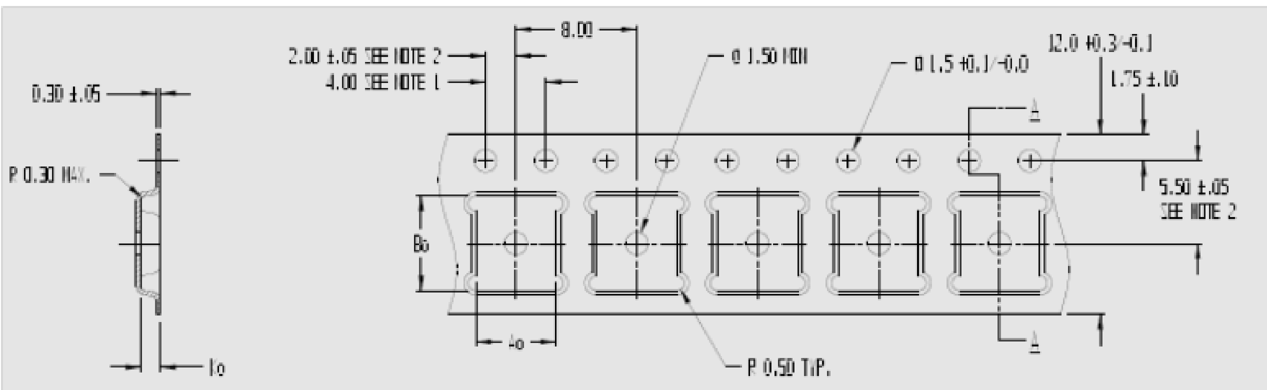
Notes:

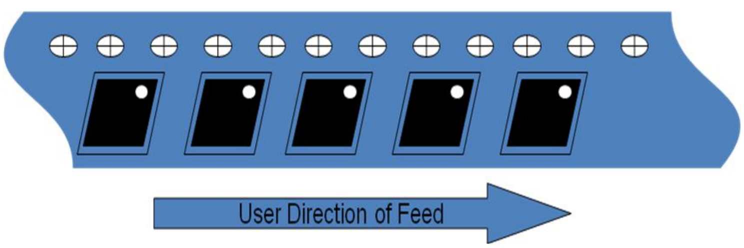
1. The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.
2. Ground vias are critical for the proper performance of this device. Vias should have a final plated thru diameter of .1524 mm (.006").
3. For best thermal performance, vias under the ground paddle should be copper filled.

Tape and Reel Information

Standard T/R size = 500 pieces on a 7” reel.

Material		Cavity (mm)				Distance Between Centerline (mm)		Carrier Tape (mm)	Cover Carrier (mm)
Vendor	Vendor P/N	Length (A0)	Width (B0)	Depth (K0)	Pitch (P1)	Length direction (P2)	Width Direction (F)	Width (W)	Width (W)
Tek-Pak	QFN0500X0 500F-L500	9.3	7.3	1.2	12.0	2.00	5.50	16.0	9.20





Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating:	Class 1A
Value:	Passed 250 V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

MSL Rating

MSL Rating:	Level 3
Test:	260°C convection reflow
Standard:	JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with lead-free soldering processes, 260 °C maximum reflow temperature.

Package lead plating: NiPdAu.

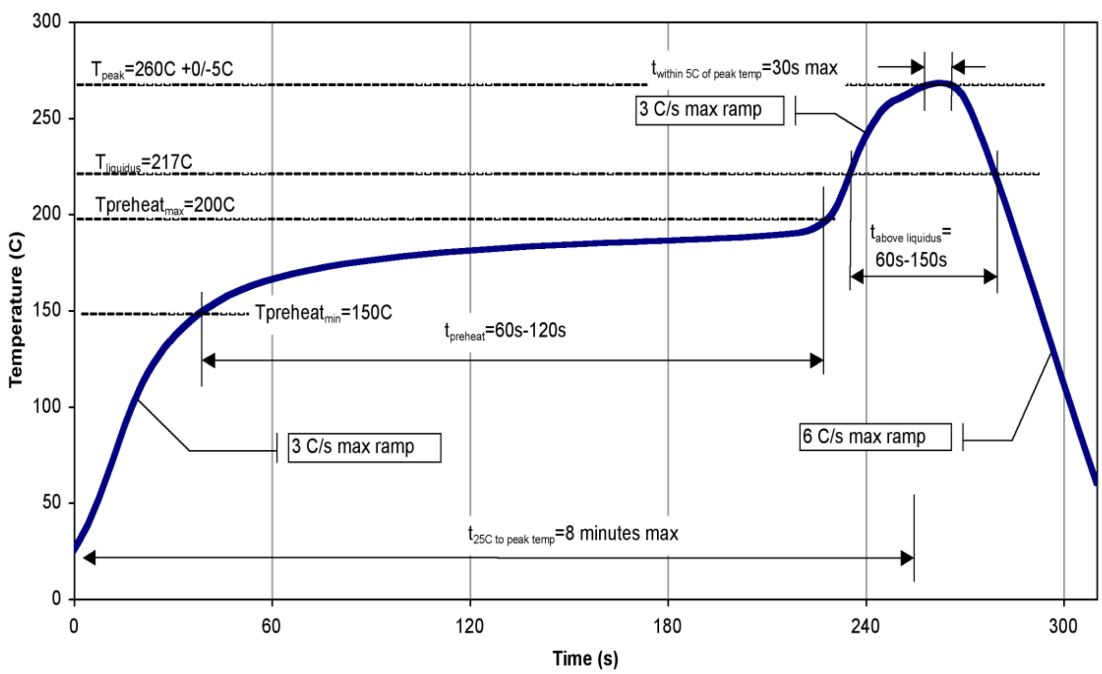
RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Recommended Solder Temperature Profile



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** +1.972.994.8465
Email: info-sales@tqs.com **Fax:** +1.972.994.8504

For technical questions and application information: **Email:** info-networks@tqs.com

Important Notice