DATA SHEET

SKY13526-485LF: 0.4 to 2.7 GHz SP6T LTE Transmit/Receive Switch with MIPI RFFE Interface

Applications

- 2G/3G/4G multimode cellular tablets and handsets (LTE, UMTS, CDMA2000, EDGE)
- Embedded data cards

Features

- Broadband frequency range: 0.4 to 2.7 GHz
- Low insertion loss
- High isolation and linearity
- External MIPI select pin
- Six linear TRX ports with isolation greater than 20 dB @ 2.7 GHz
- Small QFN (14-pin, 2 x 2 mm) package (MSL1, 260 °C per JEDEC J-STD-020)

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Description

The SKY13526-485LF is a single-pole, six-throw (SP6T) antenna switch with a Mobile Industry Processor Interface (MIPI).

Using advanced switching technologies, the SKY13526-485LF maintains low insertion loss and high isolation for both transmit and receive switching paths. The high linearity performance and low insertion loss achieved by the SKY13526-485LF makes it an ideal choice for UMTS, CDMA2000, EDGE, and LTE applications.

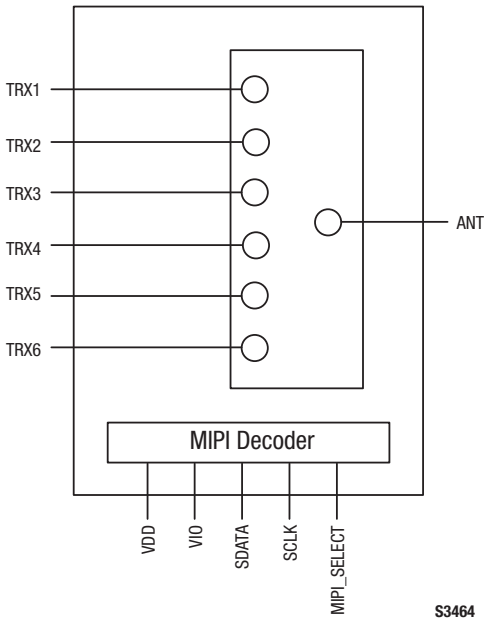


Figure 1. SKY13526-485LF Block Diagram

Depending on the logic applied to the decoder, the antenna pin is connected to one of six switched RF ports using a low insertion loss path, while the paths between the antenna pin and the other RF pins are in a high isolation state. Switching is controlled by the MIPI decoder. There is an external MIPI select pin that enables how the switch responds to power mode triggers. When this pin is grounded, the switch responds to any of the power mode triggers. When this pin is left open, the switch responds to individual power mode triggers. No external DC blocking capacitors are required on the RF paths as long as no DC voltage is applied.

The SKY13526-485LF is manufactured in a compact, 2 x 2 mm, 14-pin surface mount Quad Flat No-Lead (QFN) package.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

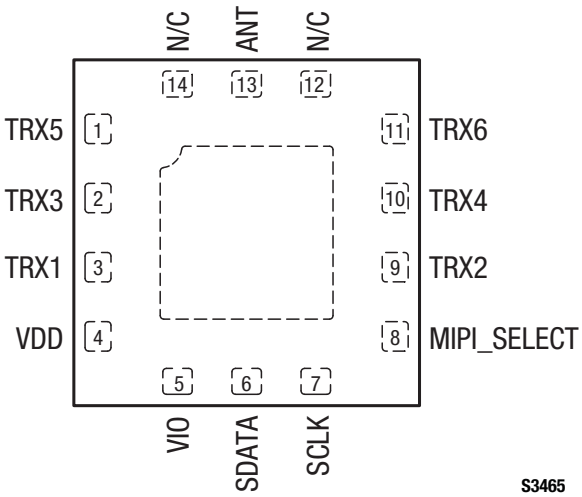


Figure 2. SKY13526-485LF Pinout – 14-Pin QFN (Top View)

Table 1. SKY13526-485LF Signal Descriptions (Note 1)

Pin	Name	Description	Pin	Name	Description
1	TRX5	RF I/O path 5	8	MIPI_SELECT	MIPI interface select. When this pin is grounded, the switch responds to any of the power mode triggers. When this pin is left open, the switch is RFFE MIPI compliant and responds to individual power mode triggers.
2	TRX3	RF I/O path 3	9	TRX2	RF I/O path 2
3	TRX1	RF I/O path 1	10	TRX4	RF I/O path 4
4	VDD	DC power supply	11	TRX6	RF I/O path 6
5	VIO	MIPI decoder interface/reference voltage	12	N/C	Not connected
6	SDATA	Data input/output	13	ANT	Antenna port
7	SCLK	Clock signal	14	N/C	Not connected

Note 1: Bottom ground paddles must be connected to ground.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY13526-485LF are provided in Table 2. Electrical specifications are provided in Tables 3 through 7.

IMD2 and IMD3 test conditions for various frequencies are listed in Tables 8 and 9, respectively.

Triple Beat Ratio (TBR) test conditions for bands 2 and 5 are listed in Table 10.

Figure 3 illustrates the test setup used to measure intermodulation products. This industry standardized test is used to simulate the WCDMA Band 1 linearity of the antenna switch. A +20 dBm Continuous Wave (CW) signal, f_{FUND}, is sequentially applied to the TRX1 through TRX6 ports, while a –15 dBm CW blocker signal, f_{BLK}, is applied to the ANT port.

The resulting 3rd Order Intermodulation Distortion (IMD3), f_{RX}, is measured over all phases of f_{FUND}. The SKY13526-485LF exhibits exceptional performance for all TRXx ports.

Table 11 describes the register content and programming read/write sequences. Refer to the *MIPI Alliance Specification for RF Front-End Control Interface (RFFE)*, v1.10 (26 July 2011) for additional information on MIPI programming sequences and MIPI bus specifications.

Figures 4 and 5 provide the timing diagrams for register write commands and read commands, respectively.

Table 12 provides the Register_0 logic. Table 13 describes the register parameters and bit values.

Table 2. SKY13526-485LF Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Minimum	Maximum	Units
Power supply	V_{DD}	2.5	5.0	V
Digital control signal, MIPI select signal	VIO		2	V
RF input power	P_{IN}		+34	dBm
Storage temperature	T_{STG}	–55	+150	°C
Operating temperature	T_{OP}	–30	+90	°C

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***CAUTION**: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 3. SKY13526-485LF General Electrical Specifications (Note 1)
(V_{DD} = 2.85 V, VIO = 1.8 V, T_{OP} = +25 °C, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Supply voltage	V_{DD}		2.50	2.85	4.80	V
Supply current, active mode	I_{DD}			35	65	µA
Supply current, low power mode	I_{DD}			10		µA
Digital control signal, MIPI select	VIO, MS		1.65	1.80	1.95	V
Interface signal: High Low			 0.8 x VIO		 0.2 x VIO	 V V
Control current: High Low					 10 5	 µA µA
Switching time				2	5	µs

Note 1: Performance is guaranteed only under the conditions listed in this table.

Table 4. SKY13526-485LF RF Electrical Specifications (Note 1)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Operating frequency	f		0.4		2.7	GHz
Insertion loss	IL	0.4 to 0.960 GHz 1.710 to 1.980 GHz 1.980 to 2.690 GHz		0.40 0.45 0.70	0.50 0.55 0.85	dB dB dB
Isolation (ANT port to any receive port) (see Table 5)	Iso	0.4 to 0.960 GHz 1.710 to 1.980 GHz 1.980 to 2.690 GHz	30 25 20	34 28 23		dB dB dB
Return loss	RL		14	20		dB
Triple Beat Ratio (also see Table 10)	TBR	650 to 900 MHz 1710 to 2155 MHz	+51 +51	+81 +81		dBc dBc
2nd Order Intermodulation	IMD2	WCDMA		–110	–102	dBm
3rd Order Intermodulation	IMD3	WCDMA		–110	–105	dBm
Large signal harmonics (P_{IN} = +25 dBm):	2fo, 3fo					
VSWR = 1:1		710 to 915 MHz 1710 to 1980 MHz 1980 to 2690 MHz		–69 –69 –69	–60 –60 –60	dBm dBm dBm
VSWR = 2:1		710 to 915 MHz 1710 to 1980 MHz 1980 to 2690 MHz		–55 –55 –55	–45 –45 –45	dBm dBm dBm

Note 1: Performance is guaranteed only under the conditions listed in this table.

Table 5. SKY13526-485LF Electrical Specifications: Insertion Loss, ANT to TRX Ports (Note 1)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

Closed Path	Frequency (MHz)	Insertion Loss (dB)					
		TRX1	TRX2	TRX3	TRX4	TRX5	TRX6
ANT-TRX	915	–0.405	–0.393	–0.398	–0.400	–0.341	–0.344
ANT-TRX	1910	–0.489	–0.489	–0.501	–0.496	–0.361	–0.398
ANT-TRX	2690	–0.708	–0.691	–0.723	–0.720	–0.545	–0.538

Note 1: Performance is guaranteed only under the conditions listed in this table.

Table 6. SKY13526-485LF Electrical Specifications: Isolation, ANT to TRX Ports (1 of 2) (Note 1)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

Closed Path	Frequency (MHz)	Isolation (dB)					
		TRX1	TRX2	TRX3	TRX4	TRX5	TRX6
TRX1	915		–39	–44	–43	–39	–45
TRX1	1910		–30	–32	–35	–32	–39
TRX1	2690		–27	–27	–31	–28	–36
TRX2	915	–43		–46	–47	–40	–45
TRX2	1910	–34		–34	–37	–32	–39
TRX2	2690	–30		–29	–32	–29	–36
TRX3	915	–52	–41		–42	–42	–45
TRX3	1910	–38	–32		–33	–32	–39
TRX3	2690	–34	–30		–29	–28	–36

Table 6. SKY13526-485LF Electrical Specifications: Isolation, ANT to TRX Ports (2 of 2) (Note 1)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

Closed Path	Frequency (MHz)	Isolation (dB)					
		TRX1	TRX2	TRX3	TRX4	TRX5	TRX6
TRX4	915	–47	–47	–39		–43	–46
TRX4	1910	–37	–34	–30		–32	–39
TRX4	2690	–33	–29	–27		–28	–36
TRX5	915	–46	–46	–48	–41		–46
TRX5	1910	–37	–35	–34	–33		–40
TRX5	2690	–33	–30	–29	–30		–36
TRX6	915	–52	–51	–47	–46	–42	
TRX6	1910	–45	–43	–40	–40	–36	
TRX6	2690	–41	–39	–36	–36	–33	

Note 1: Performance is guaranteed only under the conditions listed in this table.

Table 7. SKY13526-485LF Electrical Specifications: Isolation, TRX to TRX Ports (Note 1)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

Closed Path	Frequency (MHz)	Isolation (dB)					
		TRX1	TRX2	TRX3	TRX4	TRX5	TRX6
TRX1	915		–30	–39	–42	–50	–56
TRX1	1910		–24	–33	–35	–39	–48
TRX1	2690		–21	–28	–31	–34	–45
TRX2	915	–31		–33	–39	–47	–57
TRX2	1910	–26		–27	–32	–38	–48
TRX2	2690	–23		–23	–28	–33	–44
TRX3	915	–38	–31		–31	–42	–57
TRX3	1910	–32	–25		–25	–34	–47
TRX3	2690	–28	–22		–22	–30	–44
TRX4	915	–40	–37	–30		–32	–58
TRX4	1910	–34	–31	–24		–25	–47
TRX4	2690	–31	–27	–20		–22	–43
TRX5	915	–42	–40	–36	–31		–57
TRX5	1910	–35	–33	–30	–25		–45
TRX5	2690	–31	–29	–25	–22		–41
TRX6	915	–54	–53	–57	–58	–50	
TRX6	1910	–47	–45	–45	–47	–42	
TRX6	2690	–43	–40	–40	–42	–40	

Note 1: Performance is guaranteed only under the conditions listed in this table.

Table 8. IMD2 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker, Low (MHz)	Frequency Blocker, High (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	190	4090	–15	2140.0
2	1880.0		80	3840		1960.0
4	1732.0		400	3864		2132.0
5	836.5		45	1718		881.5
7	2535.0		120	5187		2655.0
8	897.0		45	1839		942.0

Table 9. IMD3 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	1760.0	–15	2140.0
2	1880.0		1800.0		1960.0
4	1732.0		1332.0		2132.0
5	836.5		791.5		881.5
7	2535.0		2415.0		2655.0
8	897.0		852.0		942.0

Table 10. Triple Beat Ratio Test Conditions

Band	Transmit Frequency 1 (MHz)	Transmit Power 1 (dBm)	Transmit Frequency 2 (MHz)	Transmit Power 2 (dBm)	Frequency Blocker @ ANT (MHz)	Power Blocker (dBm)	TBR Product Frequency (MHz)
2	1880.0	+21.5	1881.0	+21.5	1960.0	–30	1960.0 ± 1
5	836.5		881.5		881.5		881.5 ± 1

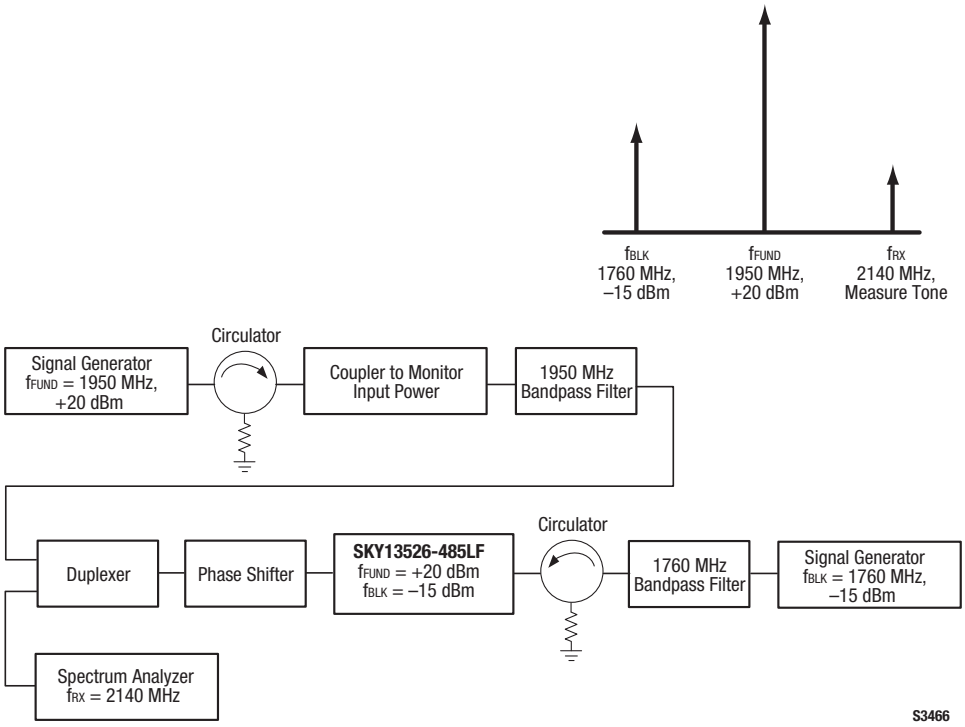


Figure 3. 3rd Order Intermodulation Test Setup

Table 11. Command Sequence Bit Definitions

Type	SSC	C11-C8	C7	C6-C5	C4	C3-C0	Parity Bits	BPC	Extended Operation					
									DA7(1)-DA0(1)	Parity Bits	BPC	DA7(n)-DA0(n)	Parity Bits	BPC
Reg0 Write	Y	SA[3:0]	1	Data[6:5]	Data[4]	Data{3:0]	Y	Y	–	–	–	–	–	–
Reg Write	Y	SA[3:0]	0	10	Addr[4]	Addr[3:0]	Y	–	Data[7:0]	–	–	–	Y	Y
Reg Read	Y	SA[3:0]	0	11	Addr[4]	Addr[3:0]	Y	Y	Data[7:0]	–	–	–	Y	Y

Legend:
SSC = Sequence start command
C = Command frame bits
DA = Data/address frame bits
BPC = Bus park cycle
BC = Byte count (# of consecutive addresses)

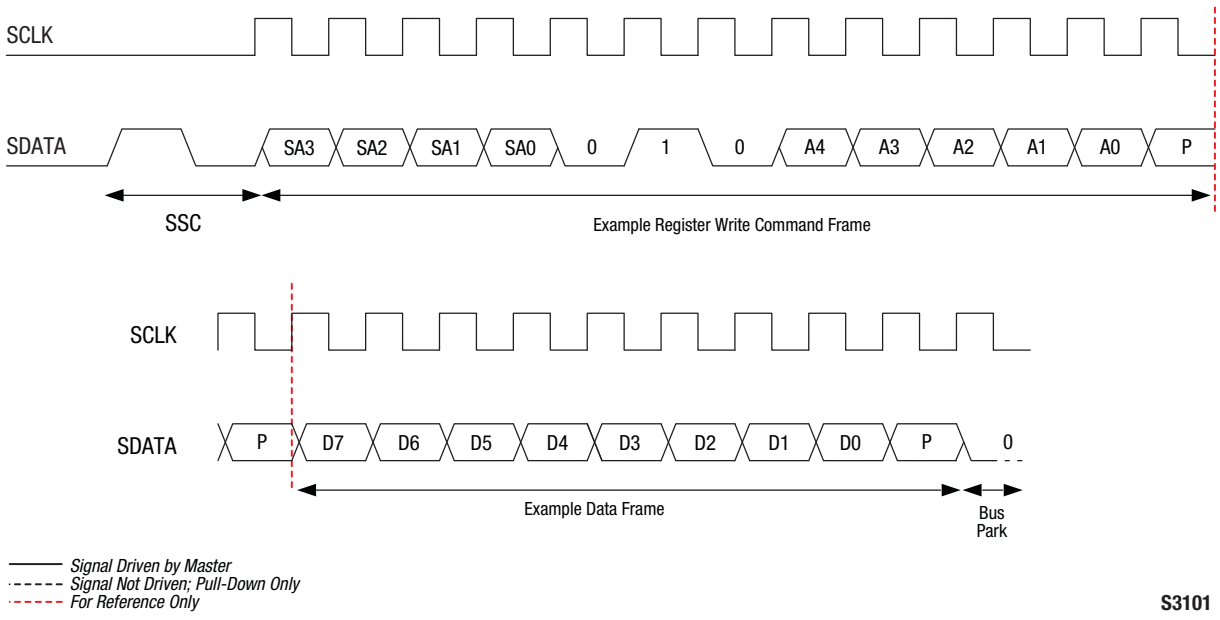


Figure 4. Register Write Command Timing Diagram

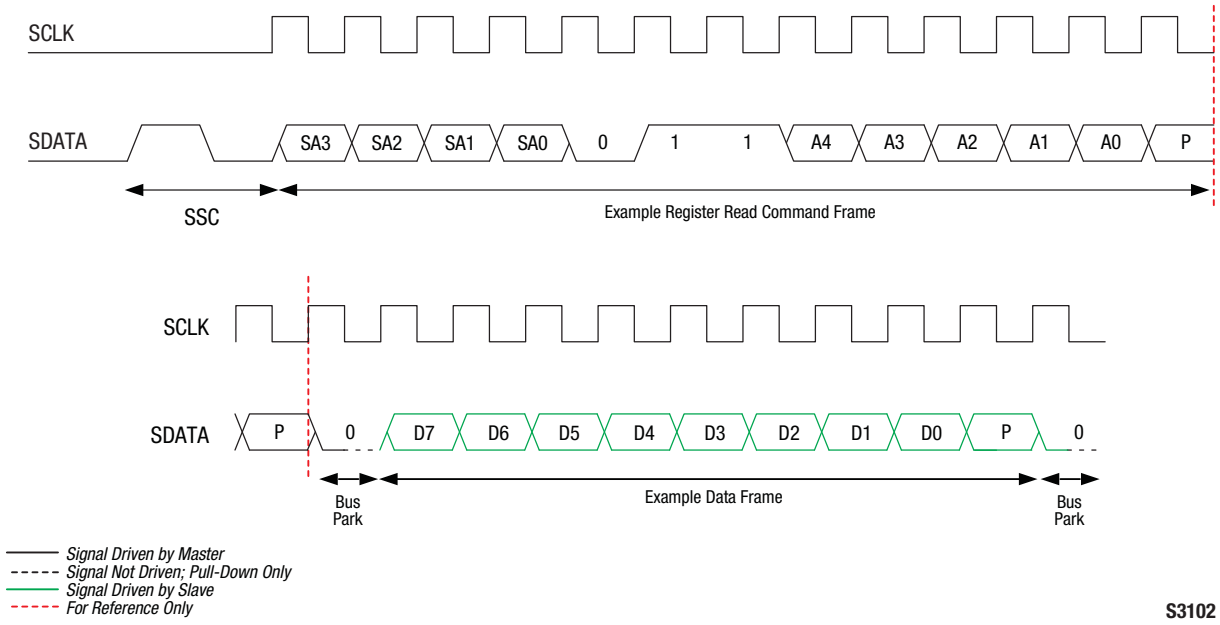


Figure 5. Register Read Command Timing Diagram

Table 12. Register_0 Truth Table

State	Mode	Register_0 Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
1	Isolation (default)	x	0	0	0	0	0	0	0
2	TRX1	x	0	0	0	0	0	1	0
3	TRX2	x	0	0	0	1	0	1	0
4	TRX3	x	0	0	0	1	1	1	0
5	TRX4	x	0	0	0	1	0	1	1
6	TRX5	x	0	0	0	0	0	0	1
7	TRX6	x	0	0	0	1	0	0	1

Table 13. Register Description and Programming (1 of 2)

Register		Parameter	Description	Default (Binary)
Name	Address (Hex)			
Register_0	0000	MODE_CTRL	Bits[7:0]: Switch control. See Table 10 for logic	–
RFFE_STATUS	001A	SOFTWARE RESET	Bit[7]: Resets all data to default values except for USID, GSID, or the contents of the PM_TRIG Register. 0 = Normal operation 1 = Software reset	0
		COMMAND_FRAME_PARITY_ERR	Bit[6]: Command sequence received with parity error – discard command.	0
		COMMAND_LENGTH_ERR	Bit[5]: Command length error.	0
		ADDRESS_FRAME_PARITY_ERR	Bit[4]: Address frame parity error =1.	0
		DATA_FRAME_PARITY_ERR	Bit[3]: Data frame with parity error.	0
		READ_UNUSED_REG	Bit[2]: Read command to an invalid address.	0
		WRITE_UNUSED_REG	Bit[1]: Write command to an invalid address.	0
		BID_GID_ERR	Bit[0]: Read command with a BROADCAST_ID (refer to the *MIPI Alliance Specification*) or GSID.	0
GROUP_SID	001B	Reserved	Bits[7:4]: Reserved	0000
		GSID	Bits[3:0]: Group slave ID	0000

Table 13. Register Description and Programming (2 of 2)

Register		Parameter	Description	Default (Binary)
Name	Address (Hex)			
PM_TRIG (Note 1)	001C	PWR_MODE	Bits[7:6]: 00 = Normal operation (active) 01 = Default settings (startup) 10 = Low power (low power) 11 = Reserved	00
		Trigger_Mask_2	Bit[5]: If this bit is set, trigger 2 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 2, the data goes directly to the destination register.	0
		Trigger_Mask_1	Bit[4]: If this bit is set, trigger 1 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 1, the data goes directly to the destination register.	0
		Trigger_Mask_0	Bit[3]: If this bit is set, trigger 0 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 0, the data goes directly to the destination register.	0
		Trigger_2	Bit[2]: If this bit is set, data is loaded into the trigger 2 registers.	0
		Trigger_1	Bit[1]: If this bit is set, data is loaded into the trigger 1 registers (unsupported).	0
		Trigger_0	Bit[0]: If this bit is set, data is loaded into the trigger 0 registers.	0
PRODUCT_ID	001D	PRODUCT_ID	Bits[7:0]: This is a read-only register. However, during the programming of the Unique Slave Identifier (USID), a write command sequence is performed on this register but the value is not changed.	11000000
MANUFACTURER_ID	001E	MANUFACTURER_ID	Bits[7:0]: Read-only register	10100101
MAN_USID	001F	Reserved	Bits[7:6]: Reserved	00
		MANUFACTURER_ID	Bits[5:4]: Read-only register	01
		USID	Bits[3:0]: Programmable USID. A write to these bits programs the USID.	1011

Note 1: Unlike the complete independence between triggers 0, 1, and 2, and also between the associated trigger masks 0, 1, and 2, respectively, as described in the MIPI RFFE Specification, this device uses additional interactions between the provided trigger functions.

The delayed application of updated data to all triggerable registers in this device may be accomplished using any of the three triggers (0, 1, or 2), provided that the particular trigger used is not currently masked off. If multiple triggers are enabled, any or all of those are sufficient to cause the data to be transferred from shadow registers to destination registers for all triggerable registers in the device.

It is also necessary to disable all three triggers (i.e., set all three trigger masks) to ensure that data written to any triggerable register will immediately be written to the destination register at the conclusion of the RFFE command sequence where the data is written.

Evaluation Board Description

The SKY13526-485LF Evaluation Board is used to test the performance of the SKY13526-485LF SP6T Switch. An Evaluation Board schematic diagram is provided in Figure 6. A recommended ESD protection circuit diagram is provided in Figure 7. An assembly drawing for the Evaluation Board is shown in Figure 8.

Package Dimensions

The PCB layout footprint for the SKY13526-485LF is provided in Figure 9. The typical part marking is shown in Figure 10. Package dimensions for the 20-pin QFN are shown in Figure 11, and tape and reel dimensions are provided in Figure 12.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY13526-485LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *PCB Design and SMT Assembly/Rework Guidelines for MCM-L Packages*, document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

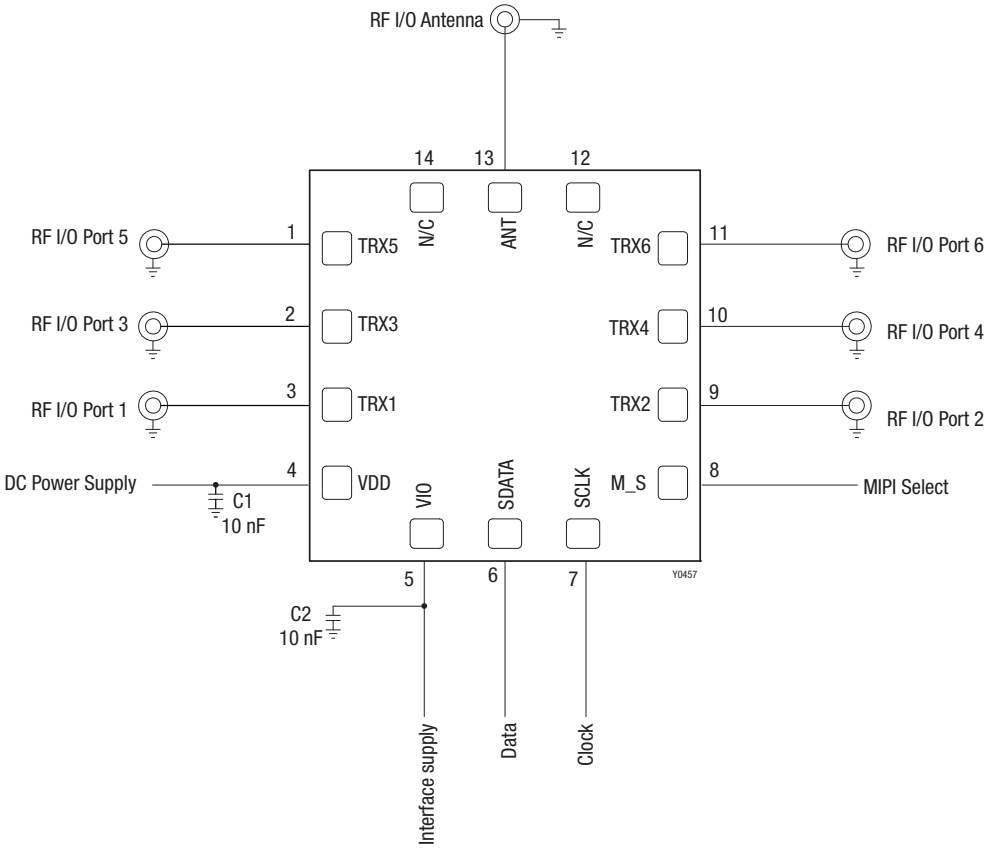
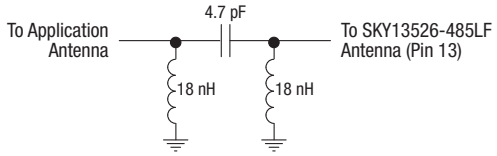
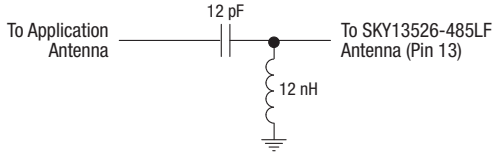


Figure 6. SKY13526-485LF Evaluation Board Schematic



ESD Circuit 1



ESD Circuit 2

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Figure 7. SKY13526-485LF Recommended ESD Protection Circuits

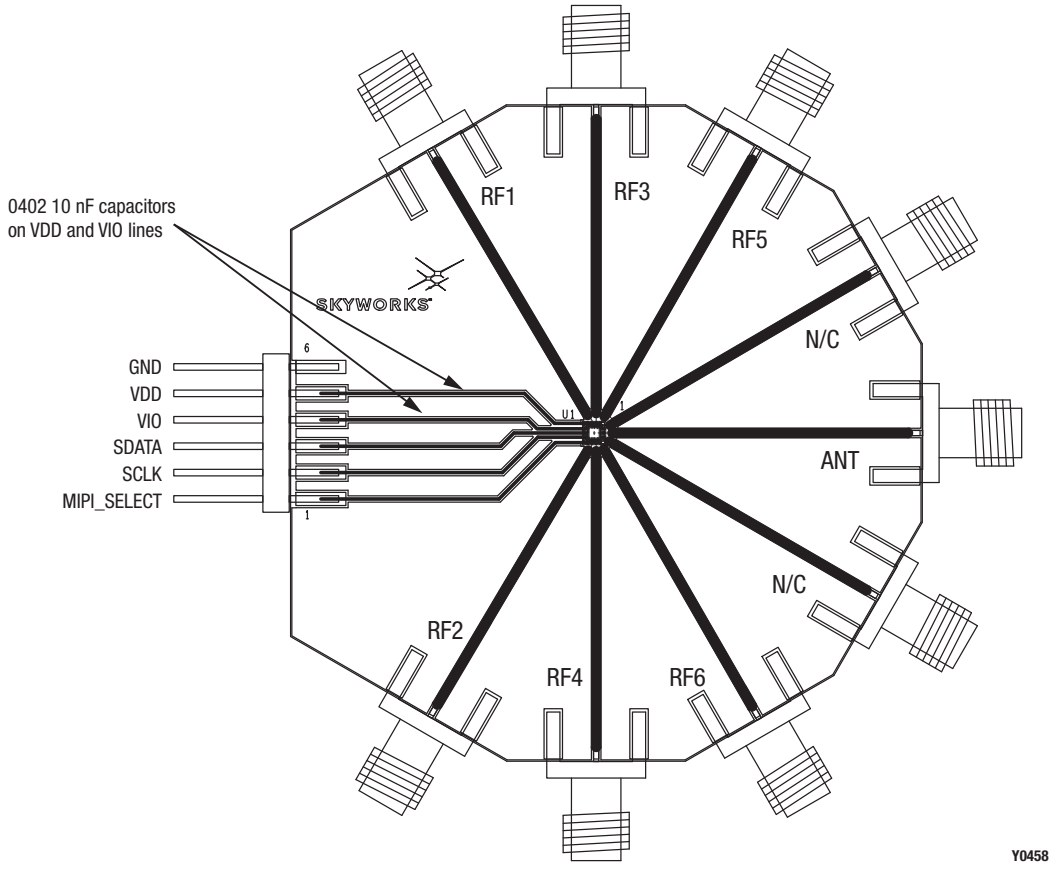

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Figure 8. SKY13526-485LF Evaluation Board Assembly Diagram

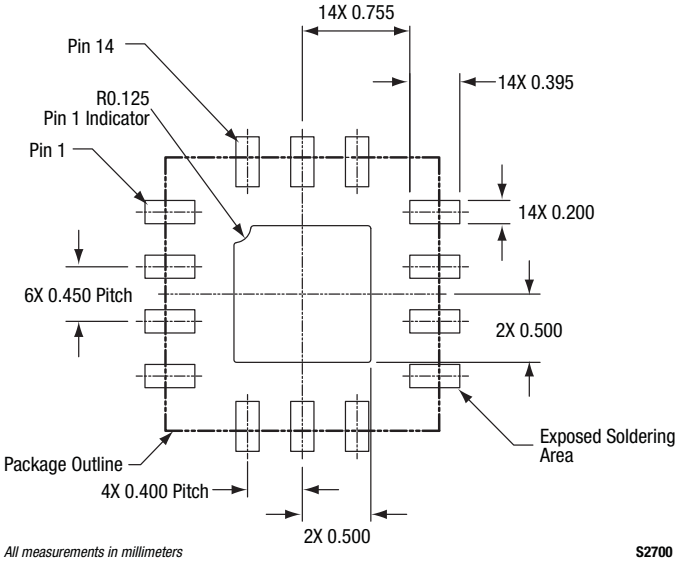


Figure 9. SKY13526-485LF PCB Layout Footprint (Top View)

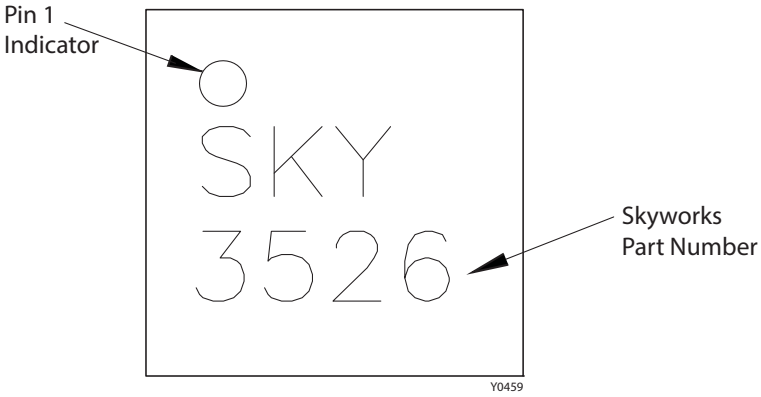
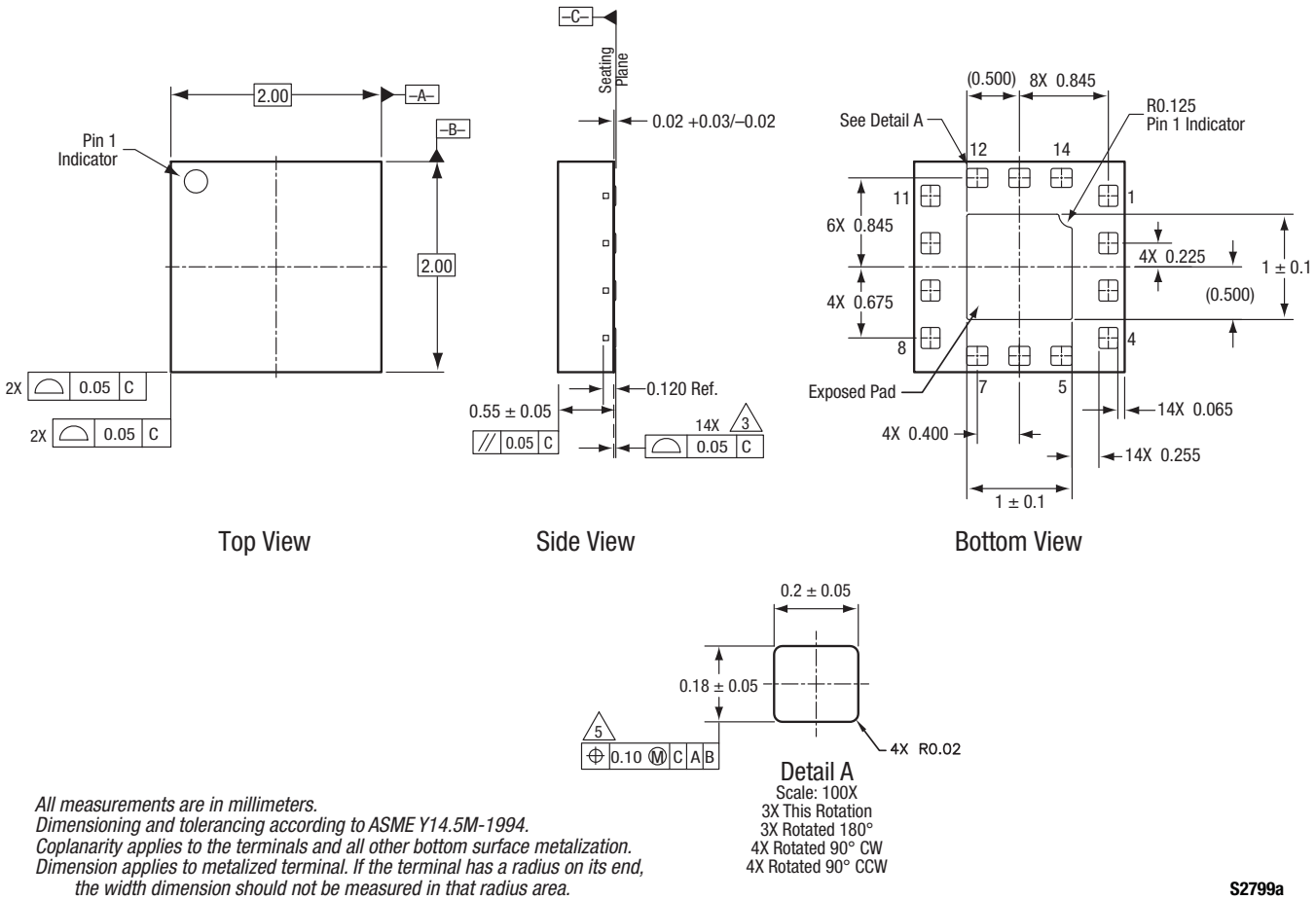


Figure 10. Typical Part Marking (Top View)



All measurements are in millimeters.
Dimensioning and tolerancing according to ASME Y14.5M-1994.
Coplanarity applies to the terminals and all other bottom surface metalization.
Dimension applies to metalized terminal. If the terminal has a radius on its end, the width dimension should not be measured in that radius area.

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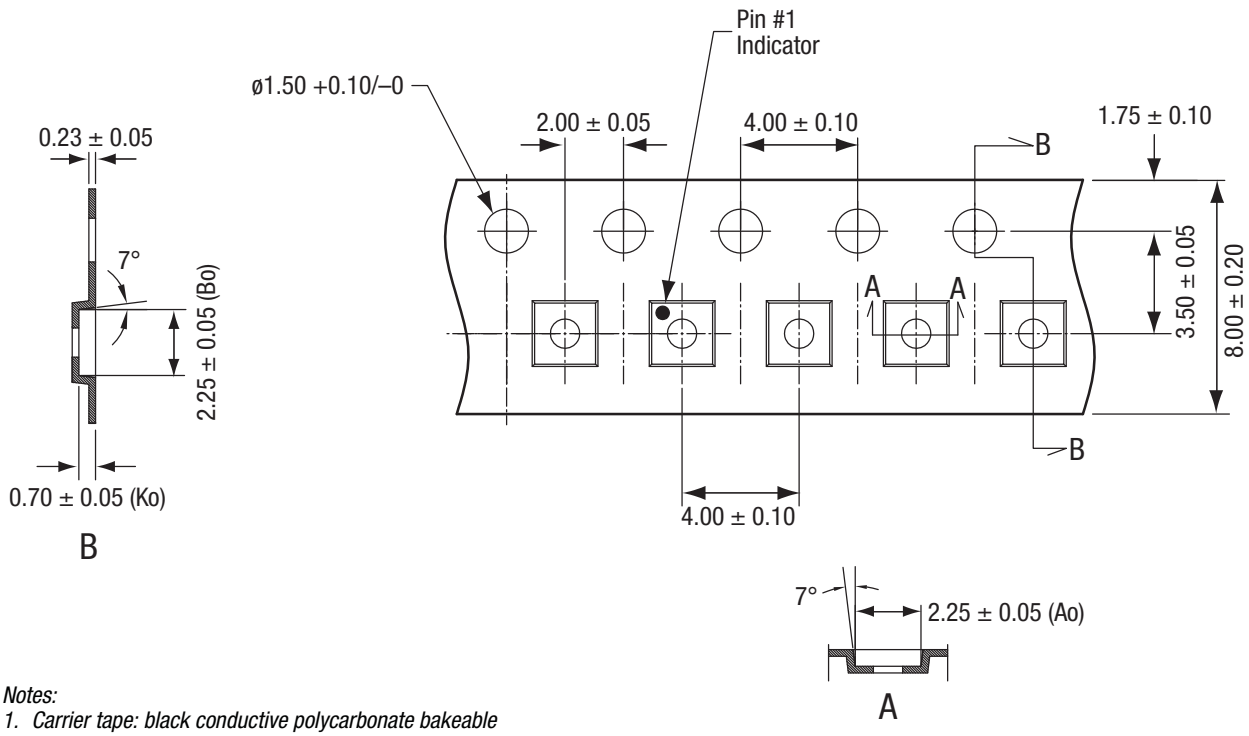
Figure 11. SKY13526-485LF 20-Pin QFN Package Dimensions



Notes:
1. *Carrier tape: black conductive polycarbonate bakeable material at 125 °C.*
2. *Cover tape material: transparent conductive with 5.40 mm width.*
3. *All dimensions are in millimeters.*

S2712

Figure 12. SKY13526-485LF Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY13526-485LF: 0.4 to 2.7 GHz SP6T LTE Transmit/Receive Switch with MIPI RFFE Interface	SKY13526-485LF	SKY13526-485LF-EVB